REMARKS

This Amendment is in response to the Office Action mailed 4, 2007». Claims 1, 4, 7-14, 17-26, 29, 30, 34-36, 39-48, 52, and 53 were pending. In this response, claims 1 XXX have been amended. No claims have been added or cancelled. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Applicants thank the Examiner for indicating that the rejections under 35 U.S.C. § 101 set forth in the previous office action have been overcome.

Rejection Under 35 U.S.C. § 103

The Examiner rejects claims 1, 4, 7-10, 12-14, 17-19, 21, 23-26, 29, 30, 34, 36, 48, 52 and 53 under 35 U.S.C. § 103(a) as being unpatentable over Rice, et al. (U.S. Patent No. 6,816,961) in view of Goodman & Miller, "A Programmer's View of Computer Architecture." Applicants respectfully disagree.

Rice describes a system that swaps bytes by selecting which field in a destination register receives which field from a source register (Rice, column 2, lines 45-51). Specifically, Rice describes a source register that includes a plurality of operation fields (Rice, column 2, lines 1-10). The fields contain two parts, a 3-bit portion and 5-bit codes that trigger the various operations (*See* Rice, column 8, Table II). Rice explicitly teaches that "five bits [are] devoted to the operation field" where a 5-bit sequence determines what operation is to be performed (Rice, column 7, lines 51-53).

Goodman describes instruction formats (Goodman, page 199). Goodman describes, at only a very high level, that a two address format for an instruction specifies that an address may act as both an addend and the address for storing a result (Goodman, page 199).

Claim 1, as amended, recites:

A method comprising:
responsive to receiving a single packed shuffle instruction designating, with 3 bits, a first register storing a first operand having a set of L data elements and designating, with 3 bits, a second register storing a second operand having a set of L control elements, wherein the first operand and second operand are of a same size and each of the L data elements and L control elements are of a same size, and wherein each one of the L control elements is divided into three portions, the first portion being a flush to zero bit occupying the most significant bit of each control element wherein the flush to zero bit alone controls whether a resultant element is flushed to zero, the second portion being a position selection field that is at least $\log_2 L$ bits wide and indicates a position of one of said L data elements, and a third portion reserved for another purpose,
storing a resultant operand in said first register having L resultant data elements of the same size as the L data elements and the L control elements to shuffle data in said first register without a modification to the L control elements of the second operand stored in the second register, wherein the value of each resultant data element is controlled by the position selection field of the L control elements in the same position as the resultant data element, and is either,
the one of the L data elements designated by the position selection field of said control element if said control element's flush to zero bit is not set; or
a zero if said control element's flush to zero bit is set.
(Emphasis Added)

The Applicants respectfully submit that Rice and Goodman, alone or in combination, fail to describe each and every feature as claimed in claim 1.

Rice describes a processing architecture that includes field swapping capability. As taught by Rice:

[A] second source register 508 includes a number of condition fields 700. Three bits of the condition field 700 is devoted to the result field select value and five bits is devoted to the operation field. The result field select bits select which source field 512 is stored in a result field 528. The operation fields are coupled to their respective operand processors 704.
(Emphasis Added) (Rice, column 7, lines 50-56)

Thus, Rice teaches that an operand specifies an address of a selected data value and an operation to be performed on that value. Furthermore, Rice explicitly states that three bits are devoted to addressing, while five bits are devoted to specifying a function to be performed. Because Rice operates on bytes of data, the addressing and function specification portions are required to occupy the entire byte of an operand. Thus, all 8 bits of each source field in Rice are taught as being devoted to only one of two purposes.

Applicants, however, claim in part:

> [E]ach one of the L control elements is divided into three portions, the first portion being a flush to zero bit occupying the most significant bit of each control element wherein the flush to zero bit alone controls whether a resultant element is flushed to zero, the second portion being a position selection field that is at least $\log_2 L$ bits wide and indicates a position of one of said L data elements, and a third portion reserved for another purpose
> (Emphasis Added)

That is, Applicants claim a control element divided into three portions each for a different purpose, with functional capabilities beyond that shown or illustrated by Rice. As such, the instruction and control element claimed by the Applicants is simply not taught or suggested by Rice. Rather, Rice explicitly teaches away from a three portion control element since Rice devotes entire bytes of source operands to only one of two purposes (*See* Rice, column 7, lines 50-56).

Furthermore, the Applicants submit that the claimed configuration is not a "matter of design choice" as previously asserted by the Examiner. The Applicants' specification recites "the 'set to zero flag' field is dominant wherein if the 'set to zero flag' field 315 is set, the rest of the fields in the mask 318 are ignored and the resultant data element position is filled with '0'" (Specification as originally filed, Paragraph [0073]). As the specification indicates, by using a

flush to zero flag which occupies the most significant bit of a control element, the remainder of the fields may be ignored without requiring the processing of such fields. Thus, in contrast to Rice, the claimed configuration is utilized for a particular purpose, which advantageously avoids unnecessarily processing data in the remaining two fields of a control element when a flush to zero has been detected. There is no indication in Rice that the operation field, which sets source field bits low, causes any processing to be ignored.

Furthermore, since Goodman merely discusses address formatting, without reference to processor instructions, control elements, or control element configurations, Goodman also must fail to teach or suggest the instruction and control element claimed by the Applicants.

The Applicants further recite "storing a resultant operand in said first register ... to shuffle data in said first register without a modification to the L control elements of the second operand stored in the second register." Thus, the instruction claimed by Applicants shuffles data in a first register without modification to the control elements in the second operand. As noted by the Examiner, Rice fails to teach or suggest a two address system (Office Action, mailed 4/04/07, page 4). The Examiner utilizes Goodman to illustrate a two address format (Office Action, page 5). However, the description in Goodman deals only with the simple addition of numbers, and not shuffling data in a register. Furthermore, Goodman fails to describe whether various addends, addresses, or variables are modified, replaced, etc. Thus, both Rice and Goodman are silent as to whether or not an operand is modified while a shuffle is performed in a first register.

Therefore, the Applicants respectfully submit that Goodman and Rice, alone or in combination, fail to describe or suggest each and every element of claim 1. Thus, claim 1 is not rendered obvious by Rice in view of Goodman, for at least the reasons noted above.

Furthermore, claims 4, 7-10, 12-14, 17-19, 21, 23-26, 29, 30, 34, 36, 48, 52 and 53 contain similar features and limitations to those discussed above with respect to claim 1. Thus, for similar reasons, claims 4, 7-10, 12-14, 17-19, 21, 23-26, 29, 30, 34, 36, 48, 52 and 53 are also not rendered obvious by Rice in view of Goodman, for similar reasons to those advanced with respect to claim 1. Therefore, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 1, 4, 7-10, 12-14, 17-19, 21, 23-26, 29, 30, 34, 36, 48, 52 and 53 under 35 U.S.C. § 103(a) as being unpatentable over Rice in view of Goodman.

The Examiner rejects claims 11, 20, 22 and 35 under 35 U.S.C. § 103(a) as being unpatentable over Rice, in view of Goodman and, further in view of the Examiner's taking of Official Notice. The Official notice, however, fails to teach or suggest the shortcomings of Rice and Goodman discussed above. Thus, Applicants respectfully requests that the Examiner withdraw the rejection of claims 11, 20, 22 and 35 under 35 U.S.C. § 103(a) as being unpatentable over Rice, in view of Goodman and, further in view of the Official Notice.

The Examiner rejects claims 39-43, 45 and 47 under 35 U.S.C. § 103(a) as being unpatentable over Rice, in view of Goodman and, further in view of Hoyle, et al. (U.S. Patent Application Publication No. 2005/0188182). Similar to the discussion above, with respect to independent claim 1, Rice and Goodman, alone or in combination, similarly fails to describe or suggest each and every element of amended independent claims 39 and 45. Hoyle discusses a system where instructions perform byte intermingling from two source operands and store a result in a third result operand (Hoyle, Abstract). Because the various three-operand byte intermingling instructions merely perform predefined intermingling operations (*See* Hoyle, Table 9), Hoyle similarly fails to teach or suggest the limitations noted above. Therefore, for reasons similar to those discussed with respect to claim 1, Rice, Goodman, and Hoyle, alone or in

combination fail to describe or suggest the limitations recited in claims 39 and 45, along with their respective dependent claims. The Applicants therefore respectfully requests that the Examiner withdraw the rejection of claims 39-43, 45 and 47 under 35 U.S.C. § 103(a) as being unpatentable over Rice, in view of Goodman and, further in view of Hoyle.

The Examiner rejects claims 44 and 47 under 35 U.S.C. § 103(a) as being unpatentable over Rice, in view of Goodman, in view of Hoyle, and further in view of the Examiner's taking of Official Notice. The Official notice, however, fails to teach or suggest the shortcomings of Rice, Goodman, and Hoyle, as discussed above. Therefore, Applicants respectfully requests that the Examiner withdraw the rejection of claims 44 and 47 under 35 U.S.C. § 103(a) as being unpatentable over Rice, in view of Goodman, in view of Hoyle, and further in view of the Official Notice.

Conclusion

Applicant reserves all rights with respect to the applicability of the doctrine of equivalents. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: October 4, 2007

By /William W. Schaal/

William W. Schaal
Reg. No. 39,018
Tel.: (714) 557-3800 (Pacific Coast)